AMENDED CLAIM SET

1   1. (currently amended) In a processor, an apparatus for issuing instructions, comprising:

2   a classification logic adapted for decoding and prioritizing instructions in relation

3   to one another and sorting said instructions in a number of priority categories;

4   a plurality of instruction queues, wherein said queues contain said instructions in

5   decoded form, wherein said plurality of said queues matches said number of said priority

6   categories, and wherein each of said queues adapted to receive only one of said priority

7   categories of said instructions from said classification logic, whereby said queues having

8   same priority categories as said instructions; and

9   an issue logic to dispatch said instructions for execution in execution units of said

10   processor, wherein said issue logic is operably coupled to said plurality of instruction

11   queues and is selecting from which of said queues to dispatch said instructions for

12   execution, wherein said issue logic has been designed to be cognizant of said priority

13   categories of said queues.

1   2. (original) The apparatus for issuing instructions of claim 1, wherein said apparatus

2   forms part of an in-order instruction issue processor architecture.

1   3. (original) The apparatus for issuing instructions of claim 1, wherein said apparatus

2   forms part of an out-of-order instruction issue processor architecture.

1   4. (original) The apparatus for issuing instructions of claim 1, wherein said plurality of

2   instruction queues consist of two queues, a high priority queue and a low priority queue.

1   5. (original) The apparatus for issuing instructions of claim 1, wherein said instructions

2   sorted in said number of priority categories by said classification logic comprise cloned

3   instructions.

1   6. (original) The apparatus for issuing instructions of claim 5, wherein said cloned

2   instructions and corresponding unmodified instructions from which said cloned

3   instructions have been derived are found in different ones of said priority category

4   queues.

1   7. (original) The apparatus for issuing instructions of claim 1, wherein said prioritizing of

2   said instructions is based on said instructions being scalar instructions or vector

3   instructions.

1   8. (original) The apparatus for issuing instructions of claim 1, wherein said prioritizing of

2   said instructions is based on a conditionality of branching.

1   9. (original) The apparatus for issuing instructions of claim 1, wherein said prioritizing of

2   said instructions is based on a probability for memory miss.

Serial No.: 10/085,606; Docket No.: YOR920020001US1   Page 4 of 10

BEST AVAILABLE COPY

1   10. (original) The apparatus for issuing instructions of claim 1, wherein said apparatus is

2   designed for prioritizing and issuing said instructions in a static manner.

1   11. (original) The apparatus for issuing instructions of claim 1, wherein said apparatus is

2   designed for prioritizing and issuing said instructions in a dynamic manner.

1   12. (original) The apparatus for issuing instructions of claim 1, wherein said apparatus

2   further comprising a predictor unit operably coupled to said classification logic, wherein

3   said predictor unit identifies performance-critical instructions.

1   13. (original) The apparatus for issuing instructions of claim 1, wherein said classification

2   logic further adapted for receiving preannotated instructions, wherein said instructions

3   have been preannotated during compilation time and said preannotations indicate said

4   priority categories.

1   14. (currently amended) In a processor, a method for issuing instructions, comprising the

2   steps of:

3   decoding and prioritizing instructions in relation to one another in a classification

4   logic;

5   sorting said instructions in a number of priority categories by said classification

6   logic;

1   providing a plurality of instruction queues for containing said instructions in

2   decoded form., wherein said plurality of said queues matching said number of said

3   priority categories, and wherein each of said queues adapted to receive only one of said

4   priority categories of said instructions from said classification logic, whereby said queues

5   having same priority categories as said instructions; and

6   selecting from which of said queues to dispatch said instructions for execution in

7   execution units of said processor by an issue logic, wherein said issue logic is operably

8   coupled to said plurality of instruction queues and, wherein said issue logic has been

9   designed to be cognizant of said priority categories of said queues.

1   15. (original) The method for issuing instructions of claim 14, wherein said method is

2   being executed in an in-order instruction issue processor architecture.

1   16. (original) The method for issuing instructions of claim 14, wherein said method is

2   being executed in an out-of-order instruction issue processor architecture.

1   17. (original) The method for issuing instructions of claim 14, wherein said step of

2   providing a plurality of instruction queues consist of providing two queues, a high priority

3   queue and a low priority queue.

1   18. (original) The method for issuing instructions of claim 14, wherein in said sorting step

2   said sorted instructions comprise cloned instructions.

1   19. (original) The method for issuing instructions of claim 18, wherein in said sorting step

2   said cloned instructions and corresponding unmodified instructions from which said

3   cloned instructions have been derived are being sorted into different ones of said priority

4   category queues.

1   20. (original) The method for issuing instructions of claim 14, wherein said prioritizing

2   step is performed based on said instructions being scalar instructions or vector

3   instructions.

1   21. (original) The method for issuing instructions of claim 14, wherein said prioritizing

2   step is performed based on a conditionality of branching.

1   22. (original) The method for issuing instructions of claim 14, wherein said prioritizing

2   step is performed based on a probability for memory miss.

1   23. (original) The method for issuing instructions of claim 14, wherein said prioritizing

2   and selecting steps are performed statically.

1   24. (original) The method for issuing instructions of claim 14, wherein said prioritizing

2   and selecting steps are performed dynamically.

1   25. (original) The method for issuing instructions of claim 14, further comprises

2   identifying performance-critical instructions with a predictor unit, wherein said predictor

3   unit is operably coupled to said classification logic.

1   26. (original) The method for issuing instructions of claim 14, further comprising the step

2   of adapting said classification logic to receive preannotated instructions, wherein said

3   instructions have been preannotated during compilation time and said preannotations

4   indicate said priority categories.

1   27. (original) A program storage device, readable by a machine, tangibly embodying a

2   program of instructions executable by the machine to perform method steps for issuing

3   instructions as recited in claim 14.